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(54) FIFO memory device for variable length data items

(57) A FIFO memory device is provided for first-in first-out storage of variable-length data items, each including a plurality of data words and a count value indicative of the number of data words in the item concerned. The device includes: a matrix (41) of storage cells for respective data words; a write pointer (43) for specifying the first row of the matrix that is available for the storage of a new data item; means (48) for extracting the word count value from a new data item to be stored; means (46) operable in dependence upon the write pointer and the extracted count value to store the successive data words of such a new data item in the cells of different columns of the specified row in a predetermined order, such storage being stopped when the number of words stored in the row reaches the count value; a read pointer (44) for specifying the row which contains the oldest data item; and (47) operable to read, in the predetermined order, the data words stored in the row specified by the read pointer. In another embodiment (Fig. 5) the device has a linear array of storage cells instead of a matrix and the reading means always read data from only the first cell of the array. After a read operation the data of the second cell is automatically shifted to the first cell and so on for all other used cells of the array.

Such FIFO memory devices permit simplification of the write control needed by a host device to store data.

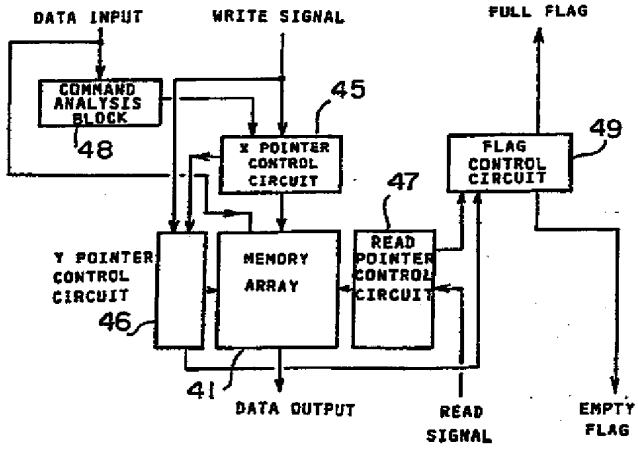

FIG. 3

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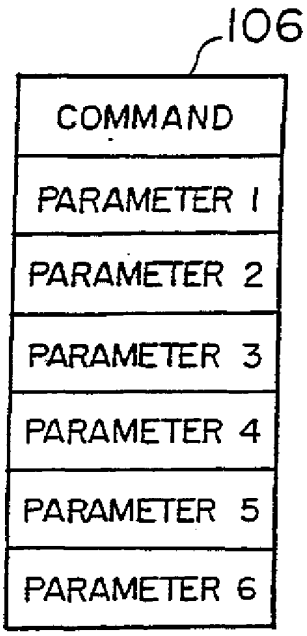
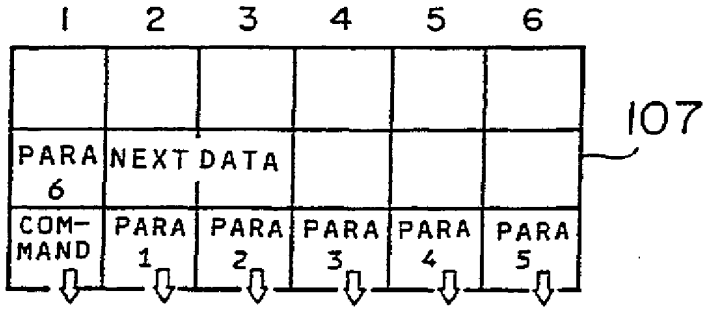
(a)



(b)



(c)

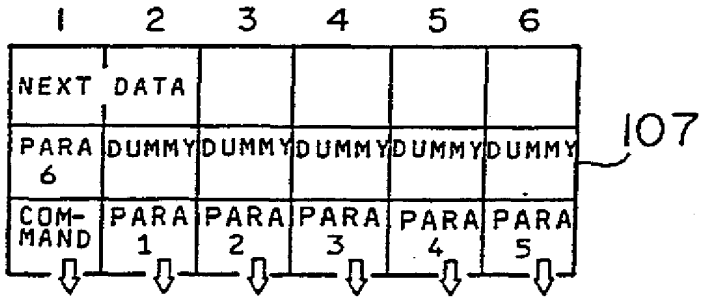


FIG. 1

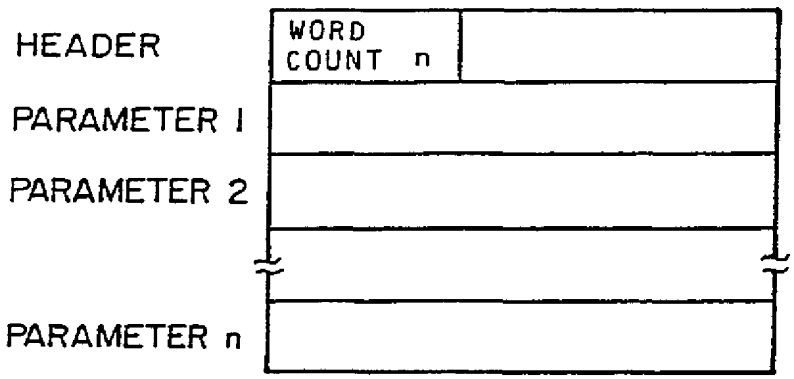


FIG. 2

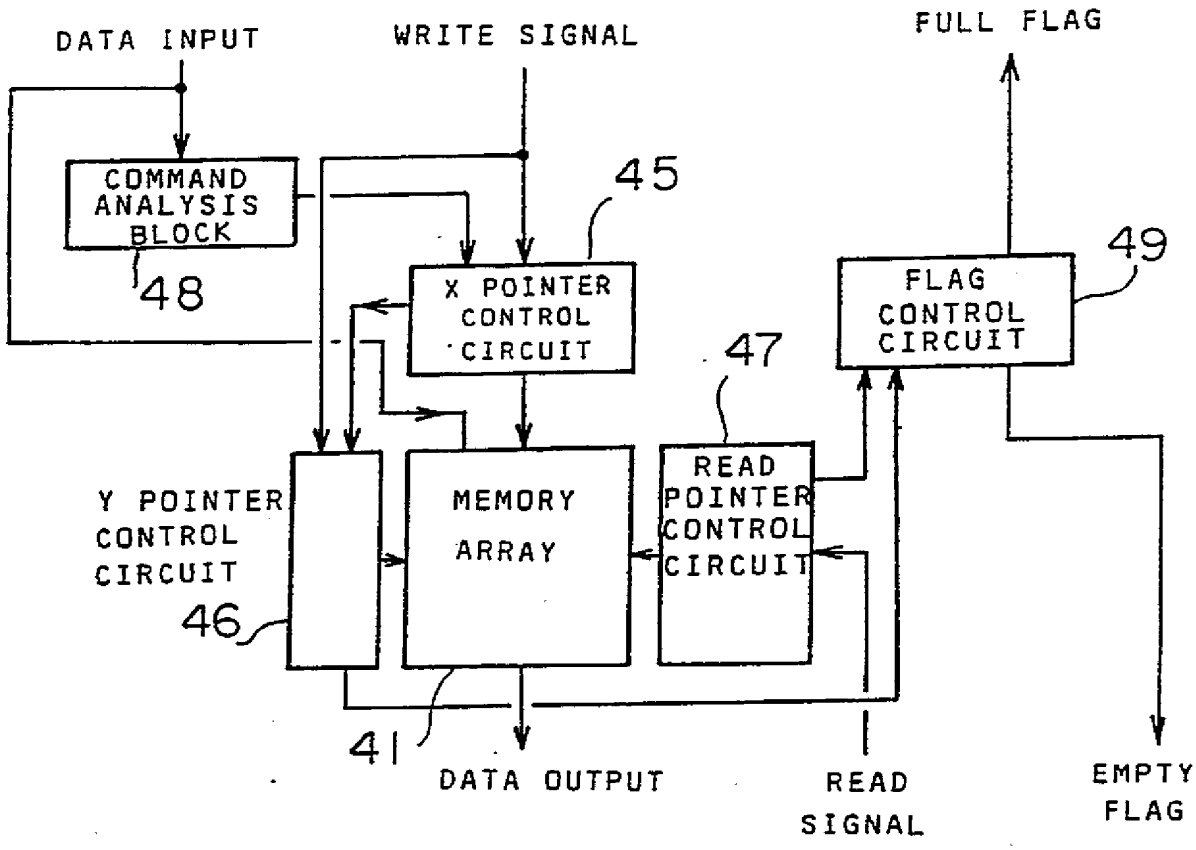


FIG. 3

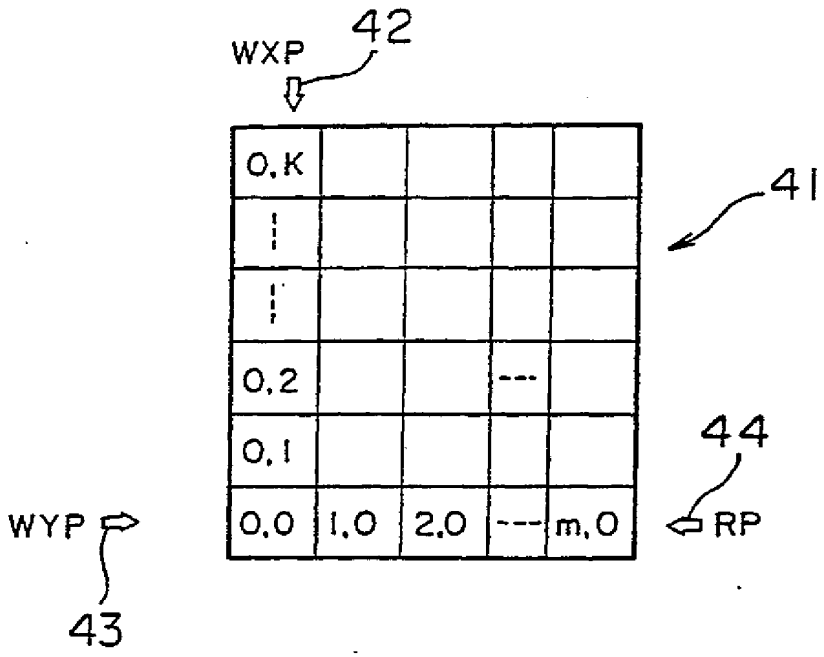


FIG. 4

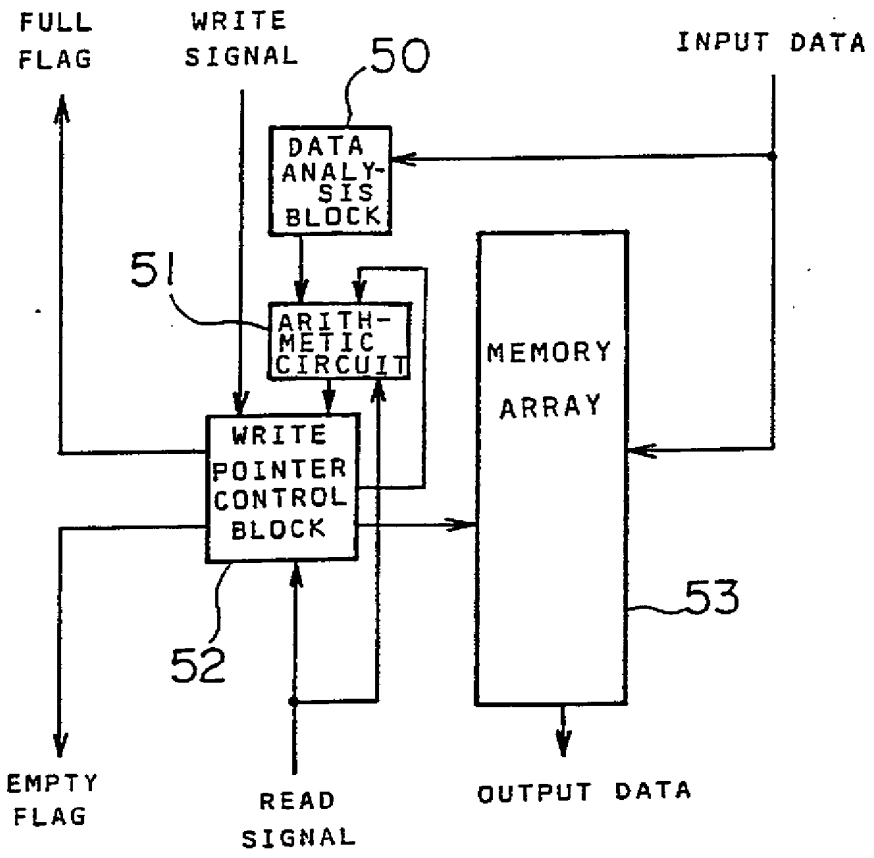


FIG. 5

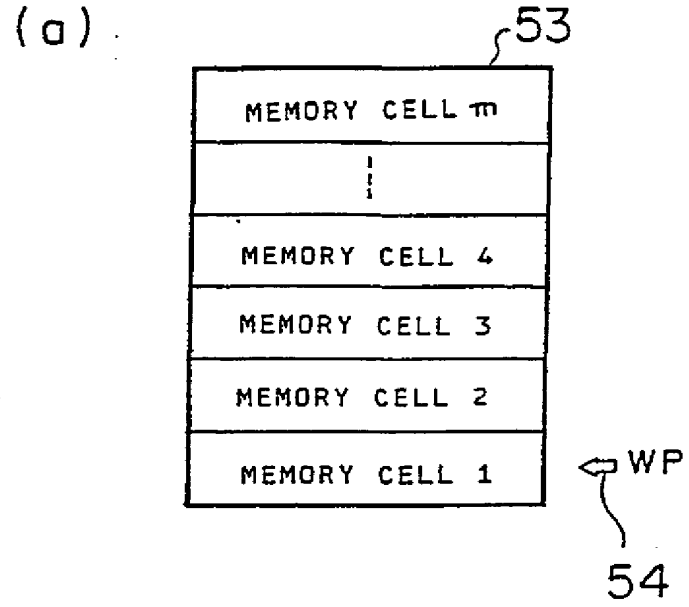


FIG. 6

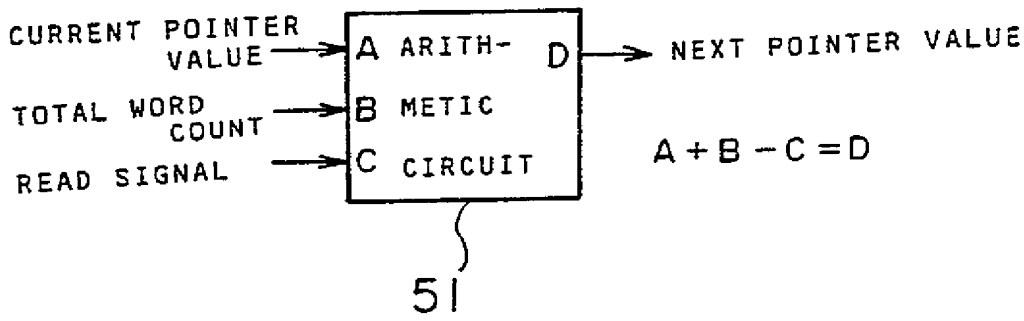


FIG. 7

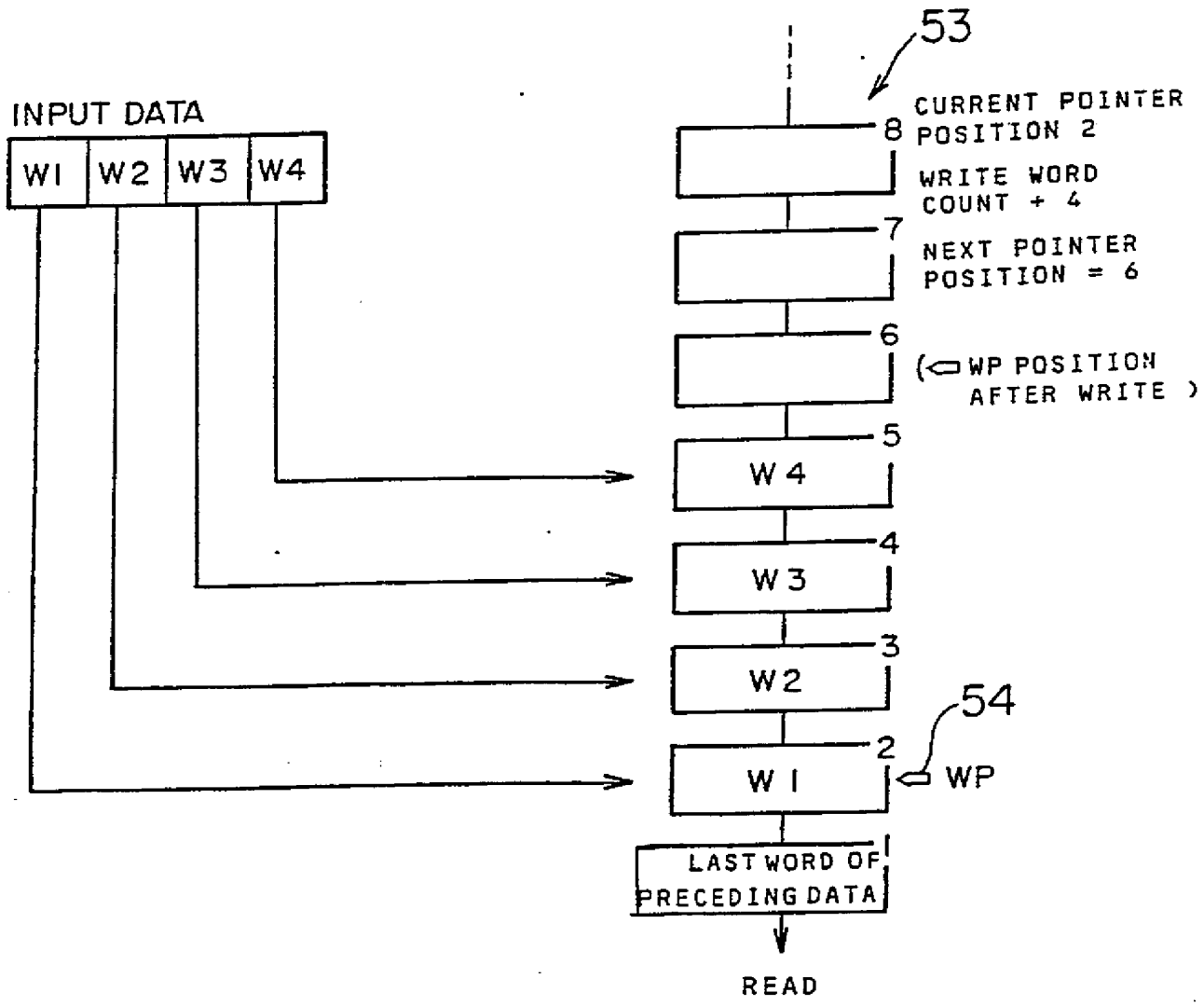


FIG. 8

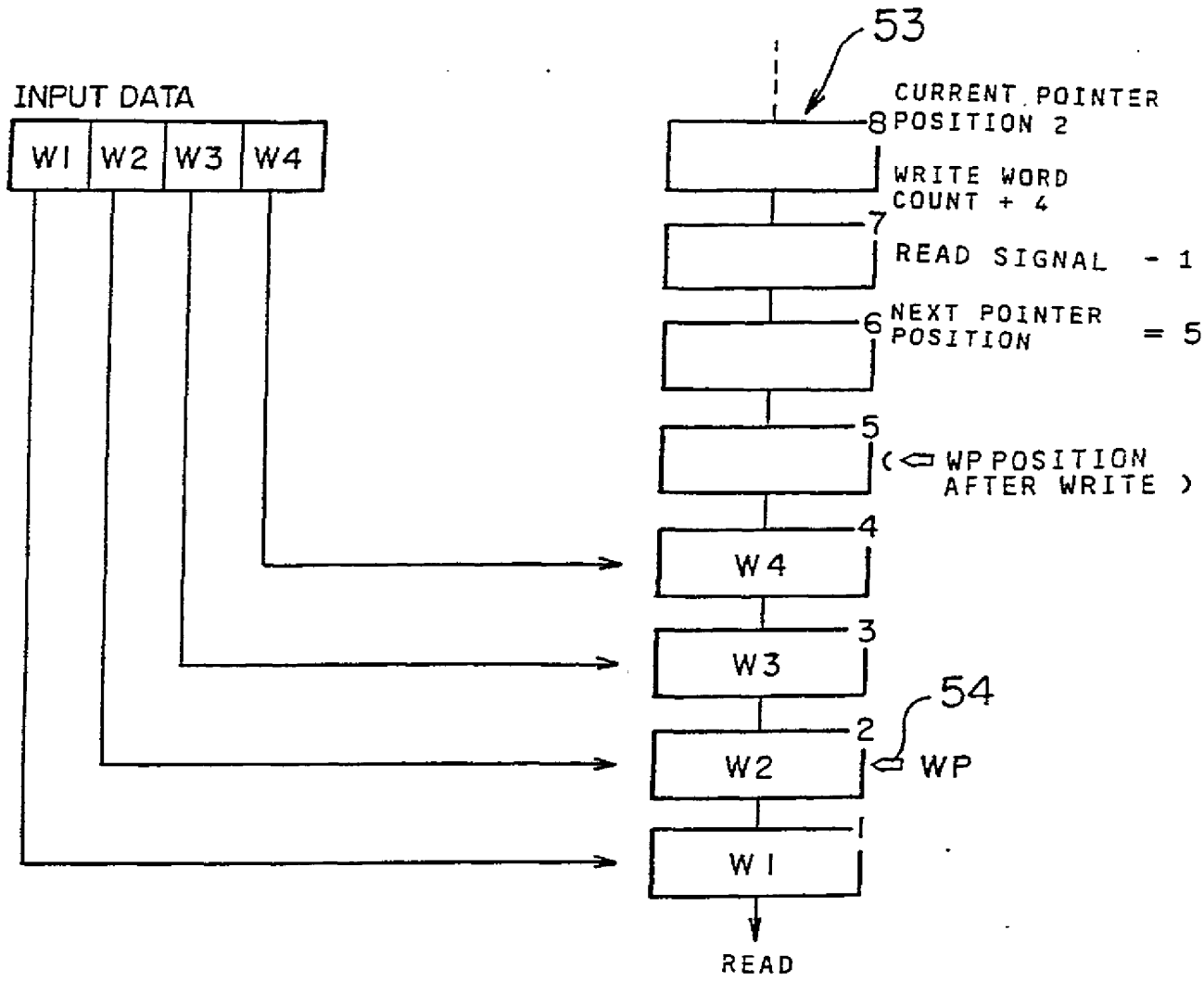

53
INPUT DATA
W1
W2
W3
W4
CURRENT POINTER POSITION 2
8
WRITE WORD COUNT + 4
7
READ SIGNAL - 1
6
NEXT POINTER POSITION = 5
5
(⇦ WP POSITION AFTER WRITE)
4
W4
3
W3
54
2
W2
⇦ WP
1
W1
READ

FIG. 9

MEMORY CELL NO.	WRITE POINTER SPECIFICATION VALUES						
	1	2	3	4	--	m - p	m-p+1
1	1	X	X	X	---	X	X
2	2	1	X	X	---	X	X
3	3	2	1	X	---	X	X
4	4	3	2	1	---	X	X
⋮	⋮	⋮	⋮	⋮		⋮	⋮
m - 1	X	X	X	X	---	p	p - 1
m	X	X	X	X	---	X	p

FIG. 10

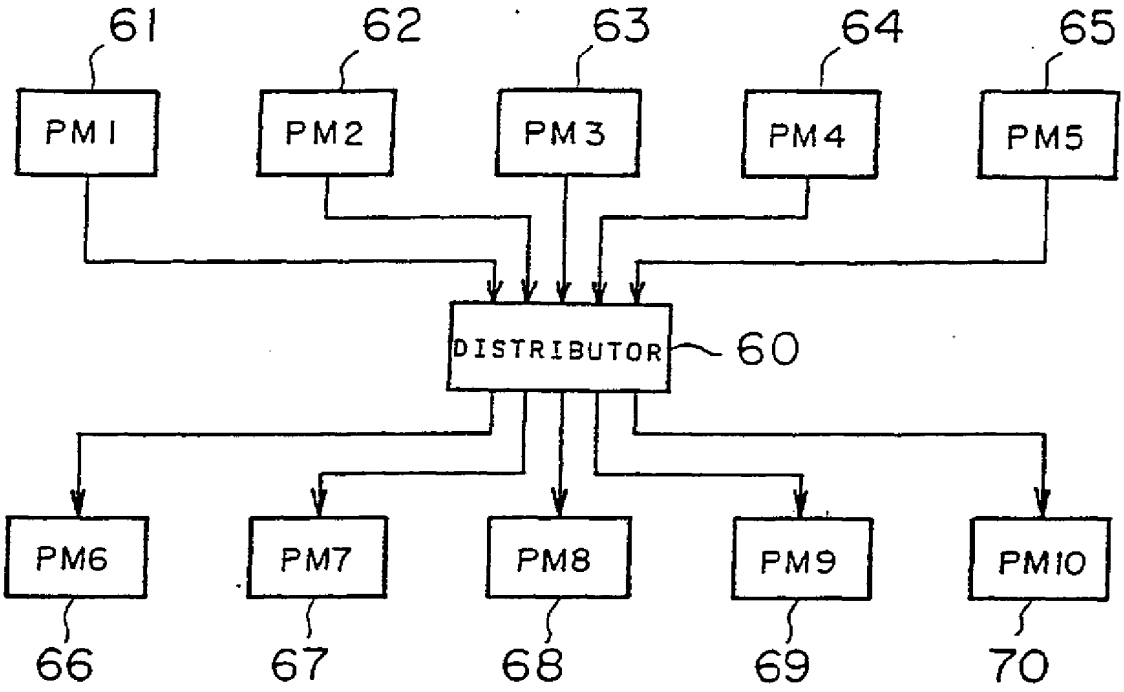


FIG. 11

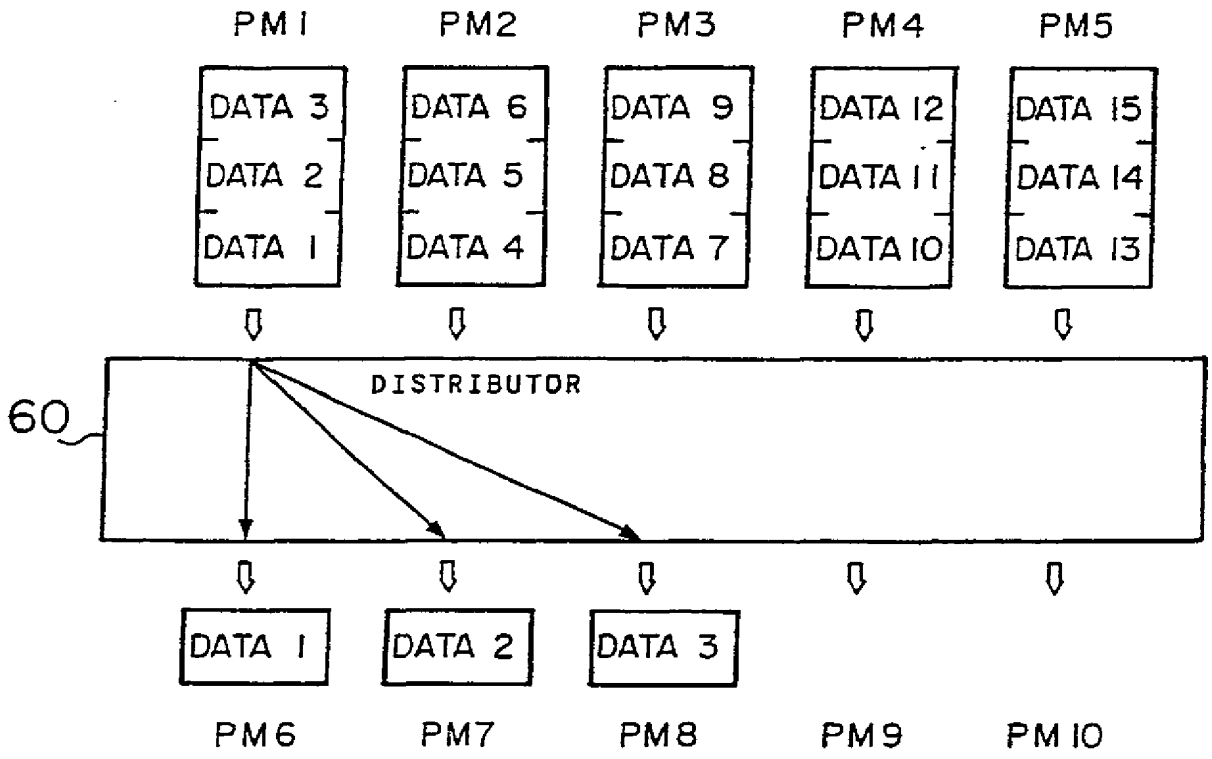


FIG. 12

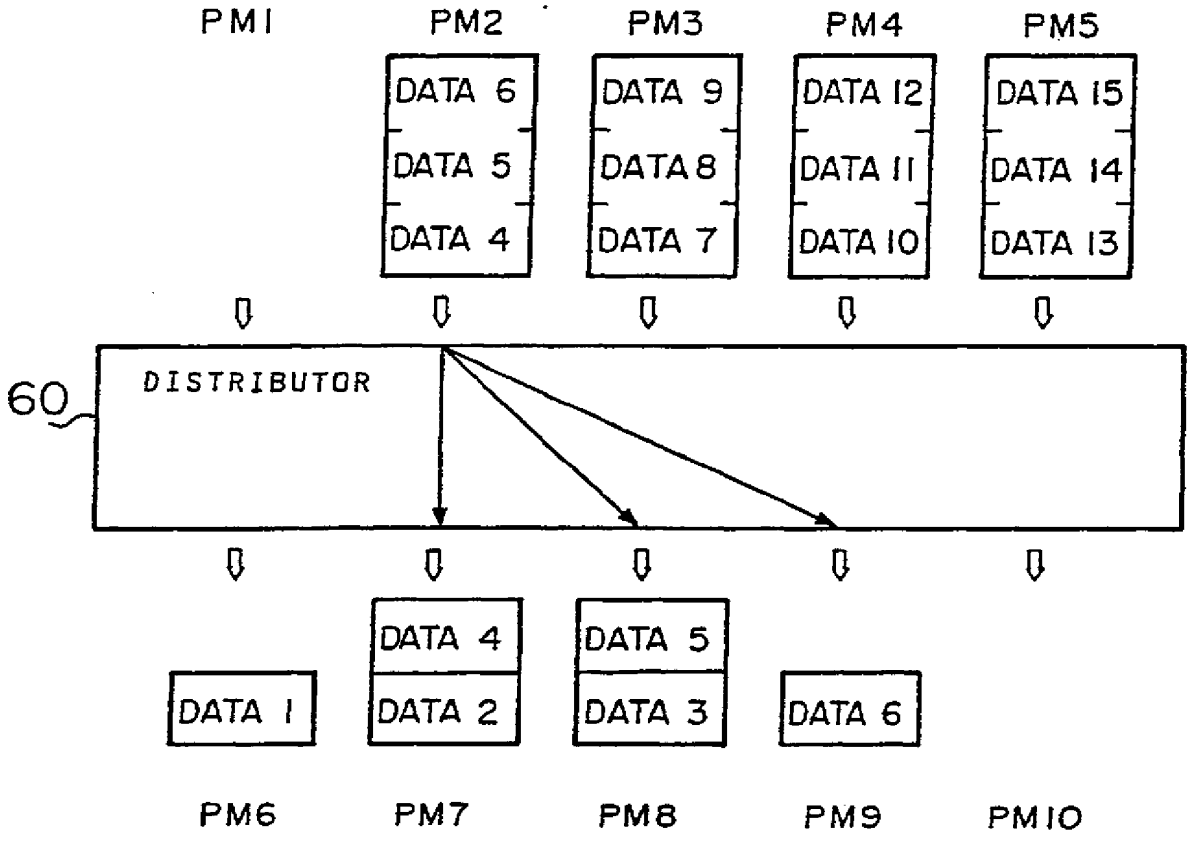


FIG. 13

FIFO MEMORY DEVICES

This invention relates to FIFO (first-in first-out) memory devices for use, for example, in image data distribution circuits, synthesizing circuits, etc., to facilitate parallel processing so as to speed up graphics processing in a three-dimensional graphics display or the like.

A memory array consisting of memory cells arrayed in rows and columns like a matrix may be used to provide a FIFO memory device in which variable-length data is input one word at a time and one data item, consisting of a plurality of words, is output in parallel at the same time; input data is written, one word at a time, starting at the beginning of each row and on the other hand, the words in all columns within one row are read out at the same time.

To enable data to be read out in such a manner, two data items are prevented from being written into the same row of the memory array. That is, if a data write operation terminates at an intermediate point of one row of the memory array, dummy data is written into the remaining columns of the row.

Figure 1 illustrates such a dummy data write operation.

Assume that an input data item 106 has, for example, an overall length of seven words, and consists of 1-word command data and 6-word parameter data, as shown in Figure 1(a), and that a memory array 107 consists of three rows x six columns of memory cells, as shown in (b) and (c).

In Figure 1, to write the input data item 106 into the memory array 107 one word at a time, parameter data 6 of the seventh word of the input data 106 is written into a memory cell on a subsequent row to the command and the parameter data 1 to 5, as shown in (b). If the next input data item is written into the memory cell

contiguous to the memory cell where the parameter data 6 is written (i.e. in further cells in the same row as the cell in which parameter data 6 of the first data item is written), output data contains the two separate data items when all columns of the row are read out simultaneously (see arrows in the figure).

To avoid this problem, dummy data is written into the remaining columns and the next data item is written into the next row, as shown in (c).

However, address control to accomplish data writing in this manner becomes complicated and consumes considerable time; this is an obstacle to speeding up graphics processing in a three-dimensional graphics display, etc.

For data read out for each row from the memory array 107, the number of bytes of one data item is unknown. Thus, when variable-length data read out is disassembled into words, dummy data other than the original words making up a data item is also handled as words.

According to a first aspect of the present invention, there is provided a FIFO memory device for first-in first-out storage of variable-length data items, each including a plurality of data words and a count value indicative of the number of data words included in the item concerned, which device includes: a matrix of individually-addressable storage cells, organised in rows and columns, for reading/writing respective data words; a write pointer for specifying the first row of the matrix that is available for the storage of a new data item; word count determining means for extracting the said count value from a new data item to be stored; writing means operable in dependence upon the write pointer and the extracted count value to store the successive data words of such a new data item in the cells of different columns of

the specified row in a predetermined order, such storage being stopped by the writing means when the number of words stored in the row reaches the extracted count value for the data item concerned; and reading means operable to read, in the said predetermined order, the data words stored respectively in the cells of that row, among the different rows of the matrix, which contains the oldest data item.

According to a second aspect of the present invention, there is provided a FIFO memory device for first-in first-out storage of variable-length data items, each including a plurality of data words and a count value indicative of the number of data words included in the item concerned, which device includes: a linear array of individually-addressable storage cells, arranged one after the next in a first direction, for reading/writing respective data words; a write pointer for specifying the first cell of the array that is available for the storage of a first word of a new data item; word count determining means for extracting the said count value from a new data item to be stored; writing means operable in dependence upon the write pointer and the extracted count value to store the first data word of such a new data item in the first-available cell specified by the write pointer and to store any further successive data words of the item in respective further cells of the array that follow the said first-available cell in the said first direction; and reading means operable to read the data word stored in the first cell of the array; the array having shift means operative, after reading of the data word stored in the said first cell of the array, to shift into that cell the data word stored in the cell of the array that immediately follows the first cell in the said first direction, and so on for all other cells of the array that currently contain data words.

In such FIFO memory devices, variable-length data can be written into each memory cell one word at a time without writing dummy data and can be read out for each data item at the same time and the read-out variable-length data can be disassembled into words correctly.

Reference will now be made, by way of example, to the accompanying drawings, in which:

Fig. 1(a) is a drawing showing an example of the format of variable-length data comprising a plurality of words;

Figure 1(b) is a drawing for explaining a data write operation, performed by a conventional FIFO memory device, for storing data having the Fig. 1(a) format;

Figure 1(c) is a drawing for explaining a dummy data write operation performed by the conventional FIFO memory device;

Figure 2 is a drawing showing the format of variable-length data;

Figure 3 is a block diagram illustrating a FIFO memory device embodying the invention;

Figure 4 is a drawing showing the arrangement of memory cells in a memory array shown in Figure 3;

Figure 5 is a block diagram illustrating another FIFO memory device embodying the invention;

Figure 6(a) is a drawing showing the arrangement of memory cells in a memory array shown in Fig. 5;

Figure 6(b) is a drawing showing in more detail a memory cell in the array of Figure 5;

Figure 7 is a drawing illustrating an operation of an arithmetic circuit shown in Figure 5;

Figure 8 is a drawing illustrating the operation of the arithmetic circuit in Figure 7 when only a write is executed;

Figure 9 is a drawing illustrating the operation of the arithmetic circuit in Figure 7 when a write and

read are executed;

Figure 10 is a drawing illustrating write pointer values when p-word input data is written into a memory array consisting of m memory cells;

Figure 11 is a block diagram showing a data distributing circuit employing the Fig. 3 and Fig. 5 embodiments;

Figure 12 is a drawing showing a first distribution step of the Fig. 11 circuit in which data provided by a processor module PM1 in Figure 11 is distributed by a distributor; and

Figure 13 is a drawing showing a second distribution step of the Fig. 11 circuit in which data provided by a processor module PM2 is distributed by the distributor.

Fig. 3 shows a FIFO memory device embodying the invention, for reading variable-length data one word at a time and outputting one data item having a plurality of words at the same time.

First, the format of variable-length data used with the Fig. 3 embodiment will be described with reference to Figure 2. Figure 2 shows one data item consisting of a header and variable-length parameter data. Each stage of the figure is one word. The header contains the total number of words of the following parameter data. In Figure 11, n is stored in the header.

In the Fig. 3 FIFO memory device, variable-length data in the format shown in Figure 2 is input to a command analysis block 48 and a memory array 41. The command analysis block 48 detects the word count n stored in the header of the input data and outputs the detected word count n to an X pointer control circuit 45.

As shown in Figure 4, the memory array 41 consists of (k+1) rows x (m+1) columns of memory cells, each for

inputting/outputting data one word at a time. The memory cell into which data is to be written is pointed to by a write X pointer (WXP) 42 and a write Y pointer (WYP) 43 (two-dimensional addressing).

On the other hand, the memory cell from which data is to be read out is pointed to by a read pointer (RP) 44 specifying only a row.. In a read operation, (m+1) words on the row pointed to by the read pointer 44 are read out at the same time.

Each time a word is written, the write X pointer 42 is incremented by one from 0 to m. When the count reaches (m+1), which is the number of columns of the memory array 41, or when the last word of one variable-length data item is written, the write X pointer 42 is reset to 0, at which time the write Y pointer 43 is incremented by one.

Returning to Figure 3, the X pointer control circuit 45 controls the count operation of the write X pointer 42 and a Y pointer control circuit 46 controls the count operation of the write Y pointer 43. A read pointer control circuit 47 controls the count operation of the read pointer 44. The X pointer control circuit 45 monitors the count value of the write X pointer 42. When the count value reaches (m+1) or (n+1) where n is the word count of variable-length input data detected by the command analysis block 48, the X pointer control circuit 45 resets the count value of the write X pointer 42 to 0.

A flag control circuit 49 compares the count value of the write Y pointer 43 with that of the read pointer 44 to determine whether write and read are enabled or disabled. When write and read are disabled, the flag control circuit 49 outputs a-full flag and an empty flag respectively.

In the Fig. 3 embodiment, the command analysis block 48 detects the word count of input variable-

length data and the X pointer control circuit 45 is responsive to the detected word count and serves to operate the write X pointer 42 for writing data. Therefore, the aforementioned dummy data write operation is not required and the control operation of the X pointer control circuit 45 is simple and can be performed at high speed, thereby speeding up graphics processing at three-dimensional graphics displays, etc.

Next, Fig. 5 shows another embodiment of the invention, for writing all words of a received variable-length data item in a single write operation and reading out one word in each read operation. Assume that the format of variable-length data used with the Fig. 5 embodiment is also as shown in Figure 2.

First, as shown in Figure 6(a), a memory array 53 consists of m rows x 1 column of memory cells, each for inputting/outputting data one word at a time. All the different words belonging to a received variable-length data item are written sequentially into the memory array 53 starting at the row pointed to by a write pointer (WP) 54 and continuing in the upward direction in the figure; data is always read out only from the memory cell on the bottom row. For this reason, just after a read operation, the word stored in each memory cell is shifted to the memory cell of the row immediately below the cell concerned. As shown in Fig. 6(b), each memory cell has one input terminal for directly writing the appropriate word of input data during a write operation and a further input terminal for writing the word stored in the memory cell of the row immediately above during a read operation.

Returning to Figure 5, a data analysis block 50 detects the word count n stored in a header of the variable-length input data having the format shown in Figure 2. An arithmetic circuit 51 calculates a new

write memory cell position of the memory array 53 to be pointed to by the write pointer after the variable-length input data has been written into the memory array 53 as described below. A write pointer control block 52 is responsive to a write signal of a write instruction and a read signal of a read instruction and serves to control the operation of the write pointer 54. The write pointer control block 52 also outputs a full flag signal and an empty flag signal as described below.

Figure 7 is an illustration of the operation of the arithmetic circuit 51. The value A of the current row pointed to by the write pointer 54, and the total word count B (which is equal to the word count n of the input data detected by the data analysis block 50 plus 1) and a value C set to 1 each time a read signal is received are input to the arithmetic circuit which then calculates A+B-C and outputs the result D as a new memory cell position of the memory array 53 to be pointed to by the write pointer 54.

Next, the operation of the Fig. 5 embodiment is described.

Figure 8 shows an example of the operation of the arithmetic circuit 51 when a write operation only is executed. Assume that the write pointer 54, before the write operation is executed, points to memory cell 2 on the second row of the memory array 53 and that a 4-word input data item is then received. In this case, the input data is written into the second to fifth rows of the memory array 53 in one write operation, and the arithmetic circuit outputs "6". Thus, the next input data will be written into rows starting at the sixth row of the memory array 53. —

Figure 9 shows an example of the operation of the arithmetic circuit 51 when both write and read operations are executed. Assume that the write pointer

54, before the write operation is executed, points to memory cell 2 on the second row of the memory array 43 and that a 4-word input data item is then received. In this case, the input data is written into the second to fifth rows of the memory array 53 in one write operation, and because one read operation is also executed, the arithmetic circuit outputs "5". Thus, the next input data will be written into rows starting at the fifth row of the memory array 53.

Even though the input data to be written in each write operation is of variable length, the write start position of the next input data to be stored is always calculated by the arithmetic circuit 51 and is pointed to by the write pointer 54. Therefore, input data is written into the memory array 53 without any gaps between the different items, and in the read operations only the original words of the received data items are handled (no dummy words are handled).

When the write pointer 54 points to memory cell 1 on the bottom row of the memory array 53, the write pointer control block 52 outputs an empty flag signal; when the number of memory cells from the current row of the memory array 53 pointed to by the write pointer to the top row is less than the word count of the next input data to the stored, the write pointer control block 52 outputs a full flag signal.

Figure 10 is a drawing for illustrating in which cells the data is stored in a write operation in which the input data consists of p words in total and the memory array 53 consists of m memory cells ($p<m$). The p-word input data is written into p memory cells starting at the memory cell having the number specified by the write pointer 54.

If the value specified by the write pointer 54 exceeds $(m-p+1)$ at the start of the write operation, not all the p-word data can be written, thus a full

flag signal is output.

The Figs. 3 and 5 embodiments can advantageously be employed together in data distributing circuits, etc., required for a three-dimensional graphics display to perform parallel processing for speeding up graphics processing.

Figure 11 is a block diagram showing a data distributing circuit using the Figs. 3 and 5 embodiments. Each processor module (PM) 61-70 has a CPU and local memory, and data calculated by the processor modules 61-65 is transferred via a distributor 60 to the processor modules 66-70 at the following stage.

Assume that data pieces provided by the processor module 61 (PM1) have been distributed to the processor modules 66, 67, and 68 (PM6, PM7, PM8) as shown in Figure 12, and that thereafter data pieces provided by the processor module 62 (PM2) have been distributed to the processor modules 67, 68, and 69 (PM7, PM8, PM9) as shown in Figure 13.

At the time, if it is necessary to distribute data 2 before data 4 and data 3 before data 5 as shown in Figure 13, the processing sequence must be specified such that distribution processing of output data from the processor module 61 is performed before that from the processor module 62; parallel processing of distribution cannot be performed.

Therefore, the processing speed of the distributor 60 is required to conform to the number of installed processor modules, in this case, the speed five times as fast as that of each of the processor modules 61-65. To provide such a high processing speed, the Figs. 3 and 5 embodiments are effective.

The distributor 60 is provided with as many of the Fig. 3 FIFO memory devices, and as many of the Fig. 5 memory devices, as there are processor modules 66-70.

Data items output from the processor modules 61-65 are distributed in the distribution processing sequence and are written into the memory arrays of the Fig. 3 memory device one word at a time. At the time, command data is added for each data item and data words are collected for each data item. After the distribution terminates, the words written into each memory array are read out at a time and are written into the memory arrays of the Fig. 5 memory devices. The data is read out from the memory arrays of the Fig. 5 memory devices one word at a time and are output to the processor modules 66-70 as one data item for each command data piece.

Distributed data is stored in the Fig. 3 FIFO memory devices in sequence for transfer to the Fig. 5 FIFO memory devices where the data is disassembled into data items for passing to the processor modules 66-70 at the following stage, thereby speeding up the processing speed of the distributor.

The foregoing is considered as illustrative only of the principles of the present invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and applications shown and described, and accordingly all suitable modifications and equivalents may be made or used provided that they fall within the scope of the invention as defined in the appended claims.

CLAIMS

1. A FIFO memory device for first-in first-out storage of variable-length data items, each including a plurality of data words and a count value indicative of the number of data words included in the item concerned, which device includes:

a matrix of individually-addressable storage cells, organised in rows and columns, for reading/writing respective data words;

a write pointer for specifying the first row of the matrix that is available for the storage of a new data item;

word count determining means for extracting the said count value from a new data item to be stored;

writing means operable in dependence upon the write pointer and the extracted count value to store the successive data words of such a new data item in the cells of different columns of the specified row in a predetermined order, such storage being stopped by the writing means when the number of words stored in the row reaches the extracted count value for the data item concerned; and

reading means operable to read, in the said predetermined order, the data words stored respectively in the cells of that row, among the different rows of the matrix, which contains the oldest data item.

2. A device as claimed in claim 1, further including a read pointer for specifying the said row, amongst the different rows of the matrix, which contains the oldest data item.

3. A device as claimed in claim 1, wherein the reading means are operative only to read from an end row of the matrix and the matrix has row shift means operative, after reading of that end row, to shift into the cells of that row the data words stored respectively in the corresponding cells of the adjacent

row of the matrix which contains the next-oldest data item, and so on for all other rows of the matrix that currently contain data items.

4. A FIFO memory device for first-in first-out storage of variable-length data items, each including a plurality of data words and a count value indicative of the number of data words included in the item concerned, which device includes:

a linear array of individually-addressable storage cells, arranged one after the next in a first direction, for reading/writing respective data words;

a write pointer for specifying the first cell of the array that is available for the storage of a first word of a new data item;

word count determining means for extracting the said count value from a new data item to be stored;

writing means operable in dependence upon the write pointer and the extracted count value to store the first data word of such a new data item in the first-available cell specified by the write pointer and to store any further successive data words of the item in respective further cells of the array that follow the said first-available cell in the said first direction; and

reading means operable to read the data word stored in the first cell of the array;

the array having shift means operative, after reading of the data word stored in the said first cell of the array, to shift into that cell the data word stored in the cell of the array that immediately follows the first cell in the said first direction, and so on for all other cells of the array that currently contain data words.

5. A device as claimed in claim 4, further including arithmetic means for adjusting the write pointer when each new data item is stored in the array in accordance

with the extracted word count for the item concerned and also when each data word is read from the first cell of the array.

6. A device as claimed in claim 5, wherein the writing means produce a full flag signal when, before the storage of a new data item, the number of available cells of the array, from the said first-available cell specified by the write pointer to the last cell of the array in the said first direction, is less than the extracted count value for that item.

7. Data distribution circuitry, for distributing variable-length data items, each including a plurality of data words and a count value indicative of the number of data words included in the item concerned, which circuitry comprises:

a first FIFO memory device, being a device as claimed in claim 1, for receiving on a word-by-word basis such variable-length data items to be distributed and storing them; and

a second FIFO memory device, being a device as claimed in claim 4, for receiving the stored data items from the first FIFO memory device and for outputting those items on a word-by-word basis.

8. A FIFO memory device substantially as hereinbefore described with reference to Figures 2 to 4, or to Figures 5 to 10 of the accompanying drawings.

9. Data distribution circuitry substantially as hereinbefore described with reference to Figures 11 to 13 of the accompanying drawings.

The Patent Office

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Application No: GB 9519123.5 **Examiner:** B.G.Western
Claims searched: 1-3, 7-9 **Date of search:** 13 October 1995

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.N): G4A AMT1

Int Cl (Ed.6): G06F 5/06

Other: On-line : WPI, INSPEC, COMPUTER

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A,E	EP-0572367-A1	TELEFONAKTIEBOLAGET L M ERICSSON (N.b pages 9-11)	-
A,P	EP-0509722-A2	NEC (See whole document)	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.